WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a die having:

a semiconductor substrate;

a plurality of device conductive regions formed in and over the substrate; and

an interconnect structure formed on the substrate to make electrical connections with the device conductive regions, and form a top surface of the die, the interconnect structure including:

a dielectric structure that contacts the substrate; and

a plurality of layers of metal that are formed in and isolated by the dielectric structure, each metal layer having a plurality of metal traces; and

a conductive region formed over the top surface of the die above the plurality of layers of metal.

2. The semiconductor device of claim 1 wherein the conductive region includes silicon.

3. The semiconductor device of claim 2 wherein the silicon is attached via an adhesive.

4. The semiconductor device of claim 2 and further comprising:

a first via that makes an electrical connection with a region of a metal trace and a first end of the conductive region; and

a second via that makes an electrical connection with a region of a metal trace and a second end of the conductive region.

5. The semiconductor device of claim 2 wherein the conductive region has a concentration of dopant atoms.

6. The semiconductor device of claim 2 and further comprising:

a dielectric region formed to contact the conductive region; and

a conductor region formed to contact the dielectric region.

7. The semiconductor device of claim 6 and further comprising:

a first via that makes an electrical connection with a region of a metal trace and the conductive region; and

a second via that makes an electrical connection with a region of a metal trace and the conductor region.

8. The semiconductor device of claim 7 wherein the conductive region has a concentration of dopant atoms.

9. The semiconductor device of claim 2 wherein the dielectric structure includes a plurality of layers, including an overlying passivation layer, the conductive region being formed over the passivation layer.

10. The semiconductor device of claim 9 and further comprising:

a plurality of contacts formed in the dielectric structure, the contacts electrically connecting the device conductive regions to the metal traces that are formed from a first layer of metal;

a plurality of vias formed in the dielectric structure, the vias electrically connecting vertically adjacent metal traces and regions; and

a plurality of pads formed in the dielectric structure, the pads being connected to a number of vias to form external points of electrical connection.

11. A method of editing a semiconductor die, the semiconductor die having:

a semiconductor substrate;

a plurality of device conductive regions formed in and over the substrate; and

an interconnect structure formed on the substrate to make electrical connections with the device conductive regions, and form a top surface of the die, the interconnect structure including:

a dielectric structure that contacts the substrate; and

a plurality of layers of metal that are formed in and isolated by the dielectric structure, each metal layer having a plurality of metal traces;

the method comprising the steps of:

forming a conductive region over the top surface of the die above the plurality of layers of metal after the die has been fabricated; and

forming a first via that makes an electrical connection with a region of a metal trace and the conductive region.

12. The method of claim 11 wherein the forming a conductive region step includes the step of forming a layer of silicon over the top surface of the die.

13. The method of claim 12 wherein the layer of silicon is connected to the top surface of the die by an adhesive.

14. The method of claim 12 and further comprising the step of forming a second via that makes an electrical connection with a region of a metal trace and the conductive region, the first and second vias being spaced apart.

15. The method of claim 14 wherein the conductive region has a concentration of dopant atoms.

16. The method of claim 12 and further comprising the steps of:

forming a dielectric region that contacts the conductive region; and

forming a conductor region that contacts the dielectric region.

17. The method of claim 12 wherein the dielectric structure includes a plurality of layers, including an overlying passivation layer, the conductive region being formed over the passivation layer.

18. The method of claim 17 and further comprising the steps of:

forming a plurality of contacts in the dielectric structure, the contacts electrically connecting the device conductive regions to the metal traces that are formed from a first layer of metal;

forming a plurality of vias in the dielectric structure, the vias electrically connecting vertically adjacent metal traces and regions; and

forming a plurality of pads in the dielectric structure, the pads being connected to a number of vias to form external points of electrical connection.

19. The semiconductor device of claim 1 wherein the conductive region is non-metallic.

20. The semiconductor device of claim 19 wherein the conductive region has a concentration of dopant atoms.